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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00202173.1

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 00202173.1
Demande n°:

Anmeldetag:
Date of filing: 22/06/00
Date de dépôt:

Anmelder:
Applicant(s):
Demandeur(s):
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Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Method of converting a series of m-bit information words to a modulated signal and vice versa, method of producing a record carrier, coding device, decoding device, reading device, signal, as well as a record carrier.

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
/

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/[redacted]
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

Title

Method of converting a series of m-bit information words into a modulated signal, method of producing a record carrier, coding device, decoding device, reading device, signal, as well as a record carrier.

Field of the invention

Method of converting a series of information words into a modulated signal, method of producing a record carrier, coding device, decoding device, recording device, reading device, signal, as well as a record carrier. The invention relates to a method of converting a series of information words to a modulated signal, in which the series of information words is converted into a series of alternate code words according to rules of conversion, so that the corresponding modulated signal satisfies predetermined criteria. The invention further relates to a method of producing a record carrier on which a signal is recorded obtained according to said method.

The invention further relates to a coding device for performing the method as claimed, this device comprising a converter for converting information words code words, means for generating a number of alternative sequences, means for selecting the alternative sequence satisfying predetermined criteria, and means for converting the selected sequence into a modulated signal.

The invention further relates to a recording device in which a coding device of this type is used. The invention further relates to a signal. The invention further relates to a record carrier on which the signal is recorded. The invention further relates to an apparatus for manufacturing said record carrier, comprising an optical system for scanning a radiation-sensitive layer of a record carrier by a radiation beam and a modulation unit for modulating the radiation beam in such a way that the pattern formed by the radiation beam in the radiation-sensitive layer corresponds to a control signal applied to the modulation unit.

The invention further relates to a decoding device for converting the signal to a series of m-bit information words, this device comprising converting means for converting the signal to a string of bits having a low or high logical

value, this bit string containing n-bit code words which correspond to the information signal portions, and this device comprising converting means for converting the series of code words to the series of information words, while a code word-dependent information word is assigned to each of the code words to be converted.

Finally, the invention relates to a reading device in which a decoding device of this type is used.

Description Relative to the Prior Art

Run length limited codes, generically designated as (*d, k*) codes, have been widely and successfully applied in modern magnetic and optical recording systems. Such codes, and means for implementing said codes, are described by K.A. Schouhamer Immink in the book entitled "Codes for Mass Data Storage Systems" (ISBN 90-74249-23-X, 1999). Run length limited codes are extensions of earlier non return to zero recording (NRZ) codes, where binarily recorded "zeros" are represented by no (magnetic flux) change in the recording medium, while binary "ones" are represented by transitions from one direction of recorded flux to the opposite direction. In a (*d, k*) code, the above recording rules are maintained with the additional constraints that at least *d* "zeros" are recorded between successive data "ones", and no more than *k* "zeros" are recorded between successive data "ones". The first constraint arises to obviate intersymbol interference occurring due to pulse crowding of the reproduced transitions when a series of "ones" are contiguously recorded. The second constraint arises in recovering a clock from the reproduced data by "locking" a phase locked loop to the reproduced transitions. If there is too long an unbroken string of contiguous "zeros" with no interspersed "ones", the clock regenerating phase-locked-loop will fall out of synchronism. In, for example, a (1, 7) code there is at least one "zero" between recorded "ones", and there are no more than seven recorded contiguous "zeros" between recorded "ones". The series of encoded bits is converted, via a modulo-2 integration operation, to a corresponding modulated signal formed by bit cells having a high or low signal value, a "one" bit being represented in the modulated signal by a change from a high to a low signal value or vice versa. A "zero" bit is represented by the lack of

change of the modulated signal. The minimum inversion period Tmin, which can be expressed by (d+1) T is thus equal to 2T where T is a bit time interval in the recording wave train. The maximum inversion period Tmax, which can be expressed by (k+1) T, is thus equal to 8T. By the way, in a train of channel bits generated by a (1, 7) code the minimum inversion period Tmin is more frequently observed than inversion periods of length 3T, 4T, etc. The fact that a lot of edge information is generated at short intervals such as 2T and 3T is advantageous to the generation of a clock signal in many cases.

As the recording density is increased, however, the minimum inversion period Tmin this time becomes a problem. That is if minimum runs 2T are generated consecutively the recording wave train is prone to distortion generated therein. This is because a 2T wave output amplitude is smaller than other wave output amplitudes and, hence, easily affected by factors such as a defocus and a tangential tilt. In addition, at a high line density, recording of consecutive minimum marks (2T) is also easily affected by disturbances such as noise. Thus, an operation to play back the data will also be prone to errors. In this case, a pattern of errors in reproduction of the data is observed as shifts of the front and rear edges of a minimum mark in many cases. As a result, the length of the generated bit error increases.

As described above, when data is transmitted through a transmission line or recorded onto a medium, the data is modulated into a coded sequence matching the transmission line or recording medium prior to the transmission or recording. If the coded sequence resulting from the modulation contains a direct current (DC) component, a variety of error signals such as tracking errors generated in control of a servo of the disc drive become prone to variations or jitter are generated easily. A first reason for using said dc-free signals is that recording channels are not normally responsive to low-frequency components. The suppression of low-frequency components in the signal is also highly advantageous when the signal is read from an optical record carrier on which the signal is recorded in the track, because then continuous tracking control undisturbed by the recorded signal is possible. A good suppression of the low-frequency components leads to improved

tracking with less disturbing audible noise. For this reason it is thus desirable to make as many efforts to prevent the modulated sequence from containing a direct current component as possible.

In order to prevent the modulated sequence from containing a direct current component, control of a DSV (Digital Sum Value) to prevent the modulated signal from containing a direct current component has been proposed. The DSV is a total found by adding up the values of a train of bits, wherein the values +1 and -1 are assigned to "1" and "0" in the train respectively, which results after NRZI modulation of a train of channel bits. The DSV is an indicator of a direct current component contained in a train of sequences. A substantially constant running digital sum value (DSV) means that the frequency spectrum of the signal does not comprise frequency components in the low frequency area. Note that DSV control is normally not applied to a sequence generated by a standard (*d, k*) code. DSV control for such standard (d, k) codes is accomplished by calculating a DSV of a train of encoded bits after the modulation for a predetermined period of time and inserting a predetermined number of DSV control bits into the train of encoded bits. In order to improve the code efficiency it is desirable to reduce the number of DSV control bits to a smallest possible value.

Preferably, the encoded signal comprises a sequence of *q* code words, where *q* is an integer. Between encoded signal portions are inserted synchronization (sync) signals. Preferably, the sync signal should not occur in a sequence of the encoded signal. Conventionally, the sync pattern contains a series of *s* consecutive bits equal to the logical "0", where *s* is an integer exceeding *k*, or alternatively the sync pattern consists of two series of *k* bits having a logical "0" separated by a bit having a logical "1", i.e. two consecutive runs of *k* "0"s. A disadvantage of the usage of such sync patterns is that they are relatively long, and therefore reduce the efficiency of the recording. Therefore, preferably, a short sync pattern is used, which may comprise a sequence of two or more consecutive "0" runs.

An example of the use of such signals to record and read an audio signal on an optical or magneto-optical record carrier can be found in United States

Patent Specification 4,501,000. The specification describes the Eight-to-Fourteen (EFM) modulation system, which is used for recording information on Compact Discs (CD) or MiniDisc (MD). The EFM-modulated signal is obtained by converting a series of 8-bit information words into a series of 14-bit code words, and where 3-bit merging words are inserted between consecutive code words. Respective code words of 14 bits satisfy the conditions that at least d=2 and at most k=10 "0"s are placed between two consecutive "1"s. In order to satisfy this condition also between code words, 3-bit merging words are used. Four 3-bit merging words of the 8 possible 3-bit merging words are permitted to be used, namely "001", "010", "000", and "100". The remaining possible 3-bit merging words, namely "111", "011", "101", and "110" are not used as they violate the prescribed d=2-constraint. One of the four allowed merging words is selected such that the bit string obtained after cascading alternate code words and merging words satisfies the (d, k)-constraint, and that in the corresponding modulo-2 integrated signal the DSV remains substantially constant. By deciding the merging words according to above rules, low-frequency (lf) components of the modulated signal can be reduced. The choice for the 3-bit merging words is based on the requirement that, on the one hand the channel signal is substantially dc-free and that also the (d, k)-constraint for the channel signal is satisfied. Decoding of EFM signals is very simple. A sync pattern is multiplexed between 33 alternative 3-bit merging words and 14-bit code words. The 27-bit sync pattern used in the CD format consists of two consecutive runs of ten "0"s plus 3-bit merging word. The choice of the merging words avoids the occurrence of said sync pattern in the output sequence. The relative occurrence of the sync pattern in this format is, 27 bits in a total of 588 bits, 4.6%. The decoder skips the 3-bit merging words, and the 14-bit code words are translated, using a look-up table or PLA etc., into the information bytes (8 bits).

Information recording has a constant need for increasing the reading and writing speed. The aim of increased reading speed, however, requires higher servo bandwidth of the tracking mechanism, which, in turn, sets more severe restrictions on the suppression of the low-frequency components in the recorded signal. Improved suppression of the low-frequency components is

also advantageous for suppressing audible noise arising from the tracking mechanism. For this reason, it is desirable to make as many efforts to prevent the signal from containing low-frequency components.

Objects and summary of the invention

It is, therefore, an object of the present invention to provide a coding system for recording data words via a (*d, k*) code, wherein the sequences generated under the rules of the (*d, k*) code have suppressed dc-components, do not generate a sync pattern, do not generate long string of 0's, and do not generate long runs of the smallest runlength *d*. This object is achieved in the coding system according to the invention, which is characterized in that the generator is embodied so as to combine mutually different digital words with the data word in order to form the alternative sequences. The digital words can be combined with the data word simply by placing the digital words in front of the data word or by placing that word in front of the digital words. Alternative different sequences are translated, using a rate *m/n*, (*d, k*) code, into alternative (*d, k*) constrained sequences from which the constrained sequence is selected with the smallest penalty, where the penalty is proportional to the dc-content and the frequency of occurrence of a plurality of undesired sub-sequences. A further object of the invention is to provide an information-recording medium such as an optical or magneto-optical disc on which digital data modulated by the invention process is recorded.

A first embodiment of the coding system according to the invention is characterized in that the generator comprises an augmentor for generating for each data word a number of intermediate sequences by combining the digital words with the data word, the generator further comprising a scrambler for scrambling the intermediate sequences in order to form the alternative sequences. The augmentor can generate the intermediate sequences simply by placing the digital words in front of the data words or by placing the data word in front of the digital words. The inclusion of the mutually different digital words in the intermediate sequences has the effect that the scrambler, which is preferably a self-synchronized scrambler, is initialized for each intermediate

sequence with a different digital word. Hence, the alternative sequences are good randomizations of the data word.

A second embodiment of the coding system according to the invention is characterized in that the augmentor is embodied so as to generate for each data word 2^r intermediate sequences by combining all possible digital words of length r with the data word. In this way a set of alternative sequences is obtained which is optimally randomized.

The above object and features of the present invention will be more apparent from the following description of the preferred embodiments with reference to the drawings, wherein:

Figure 1 shows a block diagram of an embodiment a coding system according to the invention,

Figure 2 shows an explanatory diagram of part of an embodiment of a coding scheme used for carrying out augmenting and scrambling of the digital words.

Figure 3 shows a block diagram of a selector 22 for use in a coding system according to the invention.

Figure 4 is a diagram that illustrates the general method for judging the alternative sequences.

Detailed description of the preferred embodiments

Figure 1 shows a block diagram of an embodiment of an encoding system according to the invention. Using a generator 20, a selector 22, the encoding system translates user data 19 into a (d, k) constrained sequence 23, wherein a plurality of predefined subsequences are fully absent or occur with small probability. The (d, k) constrained sequence, in turn, is translated, using a pre-coder 24, into a runlength-limited sequence 25 with suppressed low-frequency components.

As shown in Figure 1 the coding system comprises a generator 20, whose detailed block diagram is displayed in Figure 2. The generator 20 comprises an augmentor 40 that generates for each data word a number of intermediate sequences 41 by combining mutually different digital words with

the data word 19. The intermediate sequences 41 can be generated augmentor 40 simply by placing the digital words in front of the data word 19. The generator 20 further comprises a scrambler 42 that scrambles the intermediate sequences 41, one after each other, in order to form a selection set of alternative sequences 21. The inclusion of the mutually different digital words in the intermediate sequences 41 has the effect that the scrambler 42, which is preferably a self-synchronized scrambler, is initialized for each intermediate sequence 41 with a different digital word. Hence the alternative sequences 21 are relatively good randomizations of the data words 19. Preferably the augmentor is embodied so as to generate for each data word 19 2^r intermediate sequences 41 by combining all possible digital words of length *r* with the data word 19. In this way a selection set of alternative sequences 21 is obtained which is optimally randomized.

Figure 2 shows a detailed block diagram of the selector 22. The selector 22 comprises a (*d, k*) encoder 50, which translates each alternative sequence 21 into a (*d, k*) constrained sequence 51. To that end, the alternative sequence 21 is partitioned into *q m*-bit words, where *q* is an integer. Under the rules of (*d, k*) encoder 50, the *q m*-bit words are translated into *q n*-bit words, wherein *n>m*. The (*d, k*) encoder 50 can be of a standard type with parameters m=2, *n=3, d=1, k=7* or alternatively *m=1, n=2, d=2, k=7*. Preferably in order to achieve a high coding efficiency the encoder 50 has parameters *m=9, n=13, d=1*. Reference is made in this respect to the not yet published EPO application no. 99203739.0. Alternatively *m=6, n=11, d=2 or m=11, n=20, d=2*. Reference is made in this respect to the not yet published EPO application no. 00201052.8. The selector 22 further comprises means 52 that determine for each alternative (*d, k*) constrained sequence 51 if the sequence 51 contains an undesired subsequence such as the sync pattern, a long string of 0's, or a long string of alternative Tmin runs. If such an undesired sub-sequence is observed, then a judgment circuit will compute the penalty to be associated with that undesired sub-sequence. The selector 22 further comprises means 52 that judges each alternative (*d, k*) constrained sequence 51 on the number of occurrences of undesired sub-sequences such as the sync pattern, or a long string of 0's, or long string of alternative Tmin runs, and

the contribution of the alternative sequence 21 to the low-frequency components. Under the rules of the penalty algorithm, the judging means 52 gives a lower penalty for desired and a high penalty for undesired sequences. The selector 22 also comprises means 54 that selects the alternative (*d, k*) constrained sequence 51 with the lowest penalty.

Fig. 4 is a diagram that illustrates the general method used in accordance with the present invention to judge and select the alternative (*d, k*) constrained sequence 51 with the lowest penalty. As depicted in Fig. 4 the judging means 52 comprise a number of metric calculators, which measure in parallel the "0" runlength 60, the occurrence of a prescribed sync pattern 62, the alternate Tmin runlength (64), and the low-frequency content 66, respectively. The "0" runlength metric is used as a measure of consecutive "0"s (commonly referred to as a "0" runlength) detected within an alternative (*d, k*) constrained sequence 51. As discussed briefly above, when a "0" run persists within the sequence for an extended period, the recorded features such as pits and lands can become prohibitively long, which can be deleterious so that mistracking and errors are more likely to occur. The metric calculator 64 measures the number of consecutive Tmin runlength. The sync detector 62 detects if prescribed sync pattern occur in an alternative (*d, k*) constrained sequence 51. If, indeed, such a sync pattern is detected, the sync detector 62 flags that (*d, k*) constrained sequence, otherwise the sequence remains unflagged. The metric calculator 66 measures the low-frequency content of an alternative (*d, k*) constrained sequence 51. In a preferred embodiment of the present invention, the metric calculator 66 measures the DSV (Digital Sum Value) of the alternative (*d, k*) constrained sequence 51 after this sequence had been modulated using a precoding device. Preferably the variance of the DSV is measured, as it is often a more adequate measure when sequences are relatively long, exceeding100 bits. The various metrics and the sync detector flag are inputs of judging means 52. The selection means 54 finally takes a decision based on weights associated with the various input metrics of which of the alternative sequences will be selected and recorded. In the preferred embodiment of the present invention, a sync pattern is used, which consists of at least two "0" runs, which are shorter than

k. As a result, coding efficiency will benefit from such a relatively short sync pattern.

The alternative (*d, k*) constrained sequence 51 that has been selected by selector 54 is converted into a modulated signal using the NRZI pre-coding procedure. Then, the modulated signal is generated by the selected (*d, k*) constrained sequence 51 integrated modulo-2 in which a "1" becomes a transition and a "0" becomes an absence of a transition and forwarded to the recording medium.

Although the present invention has been described in detail with reference to its presently preferred embodiment, it will be understood by those of ordinary skill in the art that various modifications can be made without departing from the spirit and scope of the invention. Accordingly, it is not intended that the invention be limited, except as by the appended claims. Any reference signs do not limit the scope of the claims. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. Use of the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements.

Claims

1. A method of coding a sequence of binary data bits into a sequence of binary channel bits for recording data words onto a recordable medium via a (*d, k*) constrained code, the encoder system comprising a generator (20) for generating for each data word (19) a number of alternative sequences (21), the encoder system further comprising a selector (22) for translating each alternative sequence (21) into a (*d, k*) constrained sequence and selecting the alternative (*d, k*) constrained sequence with the lowest (in absolute sense) contribution to the DSV for recording onto the recordable medium, characterized in that the generator (20) is embodied so as to combine mutually different digital words with the data word (19) in order to form alternative sequences (21).
2. A coding method as in Claim 1, characterized in that the generator (20) comprises an augmentor (40) for generating for each data word (19) a number of intermediate sequences (41) by combining the digital words with the data word (19), the generator (20) further comprising a scrambler (42) for scrambling the intermediate sequences (41) in order to form the alternative sequences (21).
3. A coding method according to Claim 2, characterized in that the augmentor (40) is embodied so as to generate for each data word (19) 2^r intermediate sequences (41) by combining all possible digital words of length *r* with the data word (19).
4. A coding method according to any one of the Claims 1 to 3, characterized in that the selector (22) comprises a rate *m/n*, (*d, k*) constrained code for translating each alternative sequence (41) into a (*d, k*) constrained sequence (51), the selector further comprising a judgment circuit that gives a penalty proportional to the spectral content in each alternative sequence (51) and the frequency of occurrence of predefined sub sequences in the alternative sequence (51), the selector (22) also comprising means (54) for selecting the alternative (*d, k*) constrained sequence with the lowest penalty for recording onto the recordable medium.

5. A method of encoding a binary digital signal according to Claims 1, 2, 3, and 4, wherein the (*d, k*) constrained code (50) has parameters *d*=1, *m*=9, and *n*=13.
6. A method of encoding a binary digital signal according to Claims 1, 2, 3 and 4, wherein the (*d, k*) constrained code (50) has parameters *d*=2, *m*=6, *n*=11.
7. A method of encoding a binary digital signal according to Claims 1, 2, 3 and 4, wherein the (*d, k*) constrained code (50) has parameters *d*=2, *m*=11, *n*=20.
8. A method of encoding a binary digital signal according to Claims 1 to 7, wherein the sync pattern consists of at least two "0" runs shorter than k.
9. A decoder for decoding an encoded signal in accordance with method claimed in any of the preceding Claims 1 to 8.
10. An information-recording medium having recorded thereon an information structure formed in response to the method of coding as claimed in any of the Claims 1 to 8, inclusive.
11. An information recording medium according to Claims 1 to 8, wherein said information medium comprises an optically readable record carrier.
12. A coding device for carrying out the method of coding a sequence of binary data bits into a sequence of binary channel bits as claimed in any of the Claims 1 to 8, inclusive.

Abstract

This invention relates to a digital modulation method and apparatus used for recording an audio or video signal, computer data, and etc on a recording medium such as an optical or magneto-optical disc. Data words are translated into code words in accordance with a conversion table of a (d, k) code. The generated code words satisfy a (d, k) constraint in which at least d "0"s and not more than k "0"s occur between consecutive "1"s. In order to reduce the dc-components of this catenation of (d, k) constrained code words, the encoder system comprises a generator (20) and a selector (22). The generator (20) generates for each data word (19) a number of alternative sequences (21) by combining mutually different digital words with the data word (19). For this purpose, the generator (20) may comprise an augmentor (40) and a scrambler (42). The augmentor (40) generates for each data word (19) a number of intermediate sequences (41) by combining the digital words with the data word (19). The scrambler (42) scrambles these intermediate sequences (41) in order to form the alternative sequences (21). The selector 22 comprises a rate m/n, (d, k) encoder 50, which translates each alternative sequence 21 into a (d, k) constrained sequence 51. The selector 22 further comprises means 52 that computes for each alternative (d, k) constrained sequence 51 the penalty which is proportional to the frequency of occurrence of undesired sub-sequences and the contribution to the low-frequency components (dc-content). From the alternative sequences (21), the alternative sequence with the lowest penalty is selected for recording on the medium. A unique synchronising word is inserted periodically. The means for pre-coding 24 translate the chosen (d, k) constrained sequence 23 into a runlength limited sequence modulated signal 25.

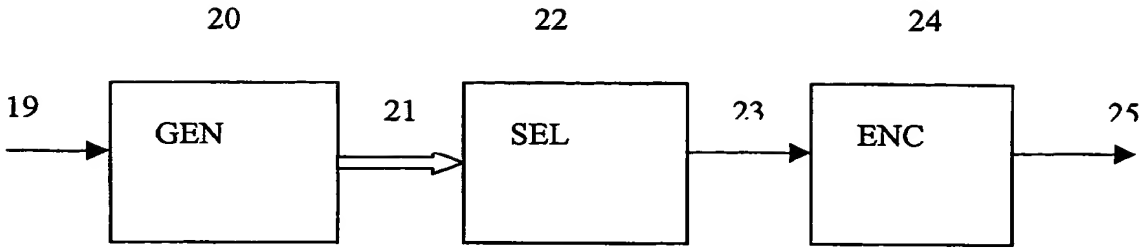

FIGURE 1

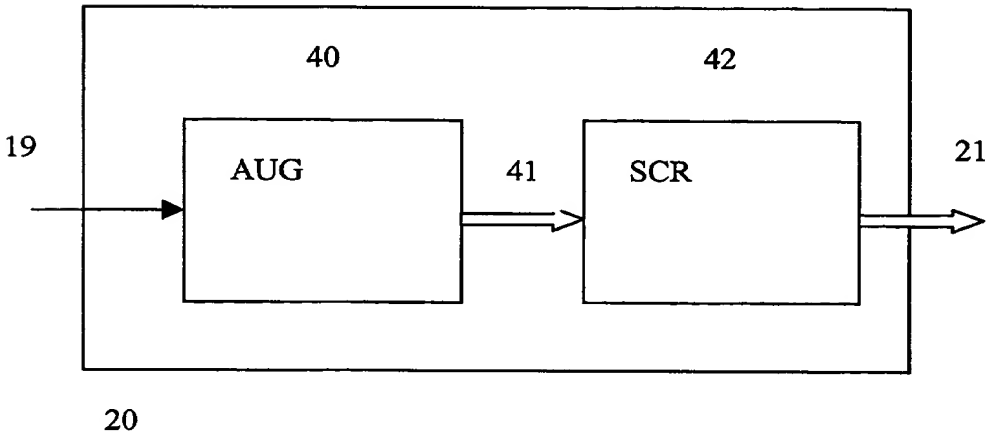

FIGURE 2

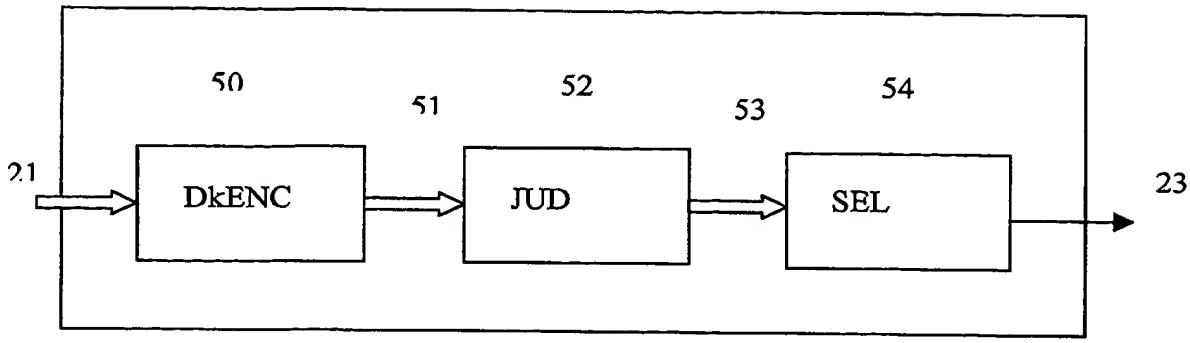

FIGURE 3

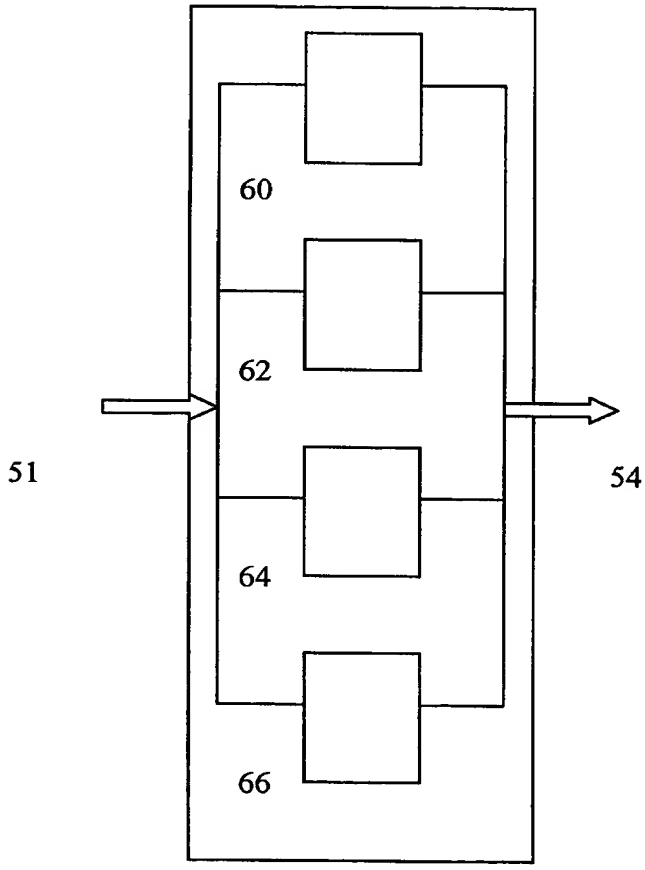

FIGURE 4